EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. David Mims on 4/7/2009.

The application has been amended as follows:

In the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method in a data processing system for synchronizing N concurrently running processes in the data processing system at a first phase before allowing the N processes to proceed to a second phase, N >= 2, comprising:

providing a first array of N elements initialized each to a first state wherein each i^{th} element of said first array is associated with an i^{th} concurrently running process which

will update the i^{th} element of the first array to a second state in response to completing the first phase, where 1 = i <= N;

providing a second array of N elements initialized each to a hold state wherein each i^{th} element of said second array is associated with the i^{th} concurrently running process associated with the i^{th} element of the first array and is used to hold the i^{th} associated concurrently running process at the first phase, and is enabled to switch, in response to receiving a release instruction, to a release state to release the i^{th} associated concurrently running process to proceed to the second phase; and

using a designated process configured to ascertain when the N elements of the first array are updated to the second state to issue the release instruction to allow the N processes to proceed to the second phase, each i^{th} process of said N concurrently running processes waits at its i^{th} associated element of said second array for said release state in response to completing the first phase and updating the i^{th} associated element of the first array; and wherein after the N elements of said first array are updated to the second state, and prior to issuance of the release instruction the N elements of said first array are reinitialized to the first state.

2. (Canceled)

3. (Currently Amended) The method recited in claim [[2]] 1, wherein each i^{th} element of

said first array has a byte size corresponding to a size of a cache line used in said data processing system.

4. (Previously presented) The method recited in claim 3, wherein each i^{th} element of said second array has a byte size corresponding to the size of said cache line used in said data processing system.

5. (Previously presented) The method recited in claim 4, wherein each i^{th} element of said second array is provided locally in relation to its i^{th} respective, associated process.

6. (Canceled)

7. (Previously presented) The method recited in claim 1, wherein the designated process is one of said N concurrently running processes.

8. (Previously presented) The method recited in claim 1, wherein the designated process is not one of the N concurrently running processes.

9. (Canceled)

10. (Previously presented) The method recited in claim 1, wherein each i^{th} element of said first array and said second array comprises a state machine.

11. (Previously presented) The method recited in claim 10, wherein said state machine is one of a counter, a gate, a flag and a sensor.

12.-13. (Canceled)

14. (Currently Amended) A system having at least one processor for processing instructions to synchronize N concurrently running processes at a first phase before allowing the N processes to proceed to a second phase, where N >= 2, the instructions comprising instructions to use:

a first array of N elements initialized each to a first state, each i^{th} element of said first array having an i^{th} concurrently running process associated therewith which will update the i^{th} element of the first array to a second state in response to completing the first phase, where 1 = i <= N;

a second array of N elements with each element initialized to a hold state wherein each i_{th} element of said second array is associated with the i^{th} concurrently running process associated with the i^{th} element of the first array and is used to hold the i^{th} associated concurrently running process at the first phase, and is enabled to switch, in response to receiving a release instruction, to a release state to release the i^{th} associated concurrently running process to proceed to the second phase;

a designated process configured to ascertain when the N elements of the first array are updated to the second state to issue the release instruction to allow the N processes to proceed to the second phase, each i^{th} process of said N concurrently running processes waits at its i^{th} associated element of said second array for said release state in response to completing the first phase and updating the i^{th} associated element of the first array; and wherein after the N elements of said first array are updated to the second state, and prior to issuance of the release instruction the N elements of said first array are reinitialized to the first state.

15. (Previously presented) The system recited in claim 14, wherein each i^{th} element of said first array has a byte size corresponding to a size of a cache line used in said data processing system.

16. (Previously presented) The system recited in claim 15, wherein each i^{th} element of said second array has a byte size corresponding to the size of said cache line used in said data processing system.

17. (Previously presented) The system recited in claim 14, wherein each i^{th} element of said second array is provided locally in relation to its respective, i^{th} associated process.

18. (Previously presented) The system recited in claim 14, wherein each i^{th} element of said first array and said second array is a state machine.

19. (Previously presented) The system recited in claim 14, wherein said state machine is one of a counter, a gate, a flag and a switch.

20.-21. (Canceled)

22. (Previously presented) The system recited in claim 14, wherein said N concurrently running processes execute on multiple processors embodied within a single computer.

23. (Previously presented) The system recited in claim 14, wherein said N concurrently running processes execute on multiple processors distributed across multiple computers connect across a network.

24 -27. (Canceled)

28. (Currently Amended) A computer program product for synchronizing N concurrently running processes in a data processing system at a first phase before allowing the N processes to proceed to a second phase, N >= 2, the computer program product comprising:

a computer useable medium having computer readable program code means embodied in the medium for synchronizing the N concurrently running processes, the computer program code means including:

computer readable program code means for providing a first array of N elements initialized each to a first state, each i^{th} element of said first array being associated with an i^{th} concurrently running process which will update the i^{th} element of the first array to a second state in response to completing the first phase, where 1 = i<= N;

computer readable program code means for providing a second array of N elements initialized each to a hold state, each i^{th} element of said second array being associated with the i^{th} concurrently running process associated with the i^{th} element of the first array and is enabled to hold the i^{th} associated concurrently running process at the first phase and to switch, in response to receiving a release instruction, to a release state to release the i^{th} associated concurrently running process to proceed to the second phase; and computer readable program code means for monitoring said first array of N elements and, in response to each i^{th} element of said first array having had its state updated, generating said instruction for switching said N elements of said second array to said release state to allow the N processes to proceed to the second phase, said computer readable program monitoring code means including computer readable program code means for processing a designated process to monitor the first array of N elements and issue the generated instruction, each i^{th} process of said N concurrently

running processes waits at its i^{th} associated element of said second array for said release state in response to completing the first phase and updating the i^{th} associated element of the first array; and wherein after the N elements of said first array are updated to the second state, and prior to issuance of the release instruction the N elements of said first array are reinitialized to the first state.

29. (Canceled)

30. (Currently Amended) A system for synchronizing N concurrently running processes at a first phase before allowing the N processes to proceed to a second phase, N >= 2, comprising:

a processor;

means for providing a first array of N elements initialized each to a first state each i^{th} element of said first array being associated with an i^{th} concurrently running process which will update the i^{th} associated element of the first array to a second state in response to completing the first phase, where $1 = i <= N$;

means for providing a second array of N elements initialized each to a hold state, each i^{th} element of said second array being associated with the i^{th} concurrently running process associated with the i^{th} element of the first array and is enabled to hold the i^{th}

associated concurrently running process at the first phase and is enabled to switch, in response to receiving a release instruction, to a release state to release the i^{th} associated concurrently running process to proceed to the second phase; and

means for monitoring said first array of N elements and, upon each i^{th} element of said first array having had its state updated, generating said instruction for switching said N elements of said second array to said release state to allow the N processes to proceed to the second phase, said monitoring means including a process designated to monitor the first array of N elements to determine when the N elements of the first array are updated to the second state and to issue the generated instruction when processed by a processor, each i^{th} process of said N concurrently running processes waits at its i^{th} associated element of said second array for said release state in response to completing the first phase and updating the i^{th} associated element of the first array; and wherein after the N elements of said first array are updated to the second state, and prior to issuance of the release instruction the N elements of said first array are reinitialized to the first state.

31. (Canceled)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-

6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
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